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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,510	01/23/2004	Dae-hoon Kwon	Q77915	5244

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EXAMINER	
JEANGLAUDE, JEAN BRUNER	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,510	KWON ET AL.	
	Examiner	Art Unit	
	Jean B Jeanglaude	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 - 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's admitted prior art (APA).

3. Regarding claim 1, The APA discloses a digital to analog converter with low skew and glitch (figs. 1 – 4) that comprises at least one current cell (11 – 14, fig. 1) (41 – 44, fig. 2)(70, fig. 4) outputting a different current amount and a current switch (the switches in figs. 1, 2) (the transistors in fig. 4) selectively enabling that at least one current cell in response to a digital signal externally supplied (page 2, lines 10 - 19), the current switch having at least one MOS transistor having an adjusted ratio so as to have a constant capacitance load regardless of the output current amounts from the at least one current cell (as noted in fig. 4, the current switch has transistors which are utilized to switch the current source 70 in order to apply the output current to the rest of the circuit) wherein the D/A converter reduces skew and glitches occurring when the at least one current cell generating different output currents is turned on and off due to the constant capacitance load (page 3, paragraphs 10, 12; fig. 3B; page 4, line 8; page 5, lines 7 – 13). Even though the APA does not explicitly disclose "a constant capacitance load". It would have been obvious to one ordinary skill in the art at the time the invention was made that the APA would perform the same function as the claim invention since upon

switching the current source current would be distributed to the circuit with different amount value and the switching the current source would allow the turn on and off due a constant capacitance load that would increase the performance of the system.

4. Regarding claim 2, the APA discloses a D/A converter (figs. 1 – 5) wherein in the at least one MOS transistor, a length L from a source to a drain of the MOS transistor times a width W formed in a vertical direction of the length L is constant regardless of the current capacities of the at least one current cell (paragraph bridging pages 6, 7).

Regarding claim 3, the APA discloses a D/A converter (figs. 1 – 4) wherein a capacitance value is a total sum of parasitic capacitances among gates and sources of the at least one MOS transistor, the gates and drains of the at least one MOS transistor and the gates and a substrate for the at least one MOS transistor (fig. 4).

1. Regarding claim 4, the APA discloses a D/A converter (figs. 1 – 5) wherein the current switches each a turn-on resistance in inverse proportion to the current capacities of the at least one current cell (figs. 1, 2, 3A).

2. Regarding claim 5, the APA discloses a D/A converter (figs. 1 – 5) that comprises a voltage controller for lowering a voltage level turning on and off the current switch to a minimum operation point of the current switch (page 5, lines 7 – 14).

3. Regarding claim 6, the APA discloses a D/A converter (fig1. 1 – 5) wherein the current switch alternately operates to form current paths for current sources between a drive voltage and a ground all the time (figs. 1 – 4).

4. Regarding claim 7, the APA discloses a D/A converter (figs. 1 – 4) wherein the at least one current cell is divided into at least two or more groups and designed for one of

the divided groups to have the same output current amount according to a thermometer type (figs. 1 – 4).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Dedic (US Patent Number 6,218,974) discloses a data multiplexing in mixed signal circuitry.

7. Dedic (US Patent Number 6,344,816) discloses a reducing jitter in mixed-signal circuitry.

8. Mercer et al. (US Patent Number RE37,619 E) discloses a skewless differential switch and DAC employing the same.

9. Volk (US Patent Number 6,369,734) discloses a method and apparatus for increasing linearity and reducing noise coupling in a DAC.

10. Bugeja et al. (US Patent Number 6,417,793) discloses a track/attenuate circuit and method for switched current source DAC.

11. Volk (US Patent Number 6,496,132) discloses a method and apparatus for increasing linearity and reducing coupling in a DAC.

12. Khoini-Poorfard et al. (US Patent Number 6,639,534) discloses a DAC switching circuitry.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B Jeanglaude whose telephone number is 571-

272-1804. The examiner can normally be reached on Monday - Friday 7:30 A. M. - 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean Bruner Jeanglaude
Primary Examiner
October 05, 2004